

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
DDR III DIMM 1 ,DDR III DIMM 2	7,8
CP-PCI/E/DMI/USB/CLK	9
CP-SATA/HOST/FAN/GPIO/VGA	10
CP-SMB/LPC/AUDIO/RTC/RST	11
CP-POWER,GND/NVRAM	12,13
CP STRAPS	14
PCI E x1 Slot / SDVO Connector	15
SIO-Fintek F171808A	16
VGA	17
EDP	18
HDMI	19
LAN-Lewisville 82579	20
Audio Codec ALC889	21
USB Connector	22
SATA / FAN Control	23
ACPI Controller UPI	24
CP / CPU_SA Power	25
DDR Power - uP6103 1-Phase	26
CPU_VTT - ISL95870B- 1-Phase	27
VRD12 - ISL6364CR+ 1Phase	28
VCCP ABD CPU_GFX POWER	29
ATX F_Panel/TPM	30
Manual Parts	31
CPU/PCH XDP	32
History	33

MS-7677 Mini ITX Ver: 1.0

Intel -SugarBay plamform

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point

OnBoard Chipset:

HD Audio Codec:RTL889

LAN-Lewisville 82579

SIO:Fintek F171808A

Flash ROM: 64 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X1) Slot * 1

PWM:

VRD12 - ISL6364CR+1Phase

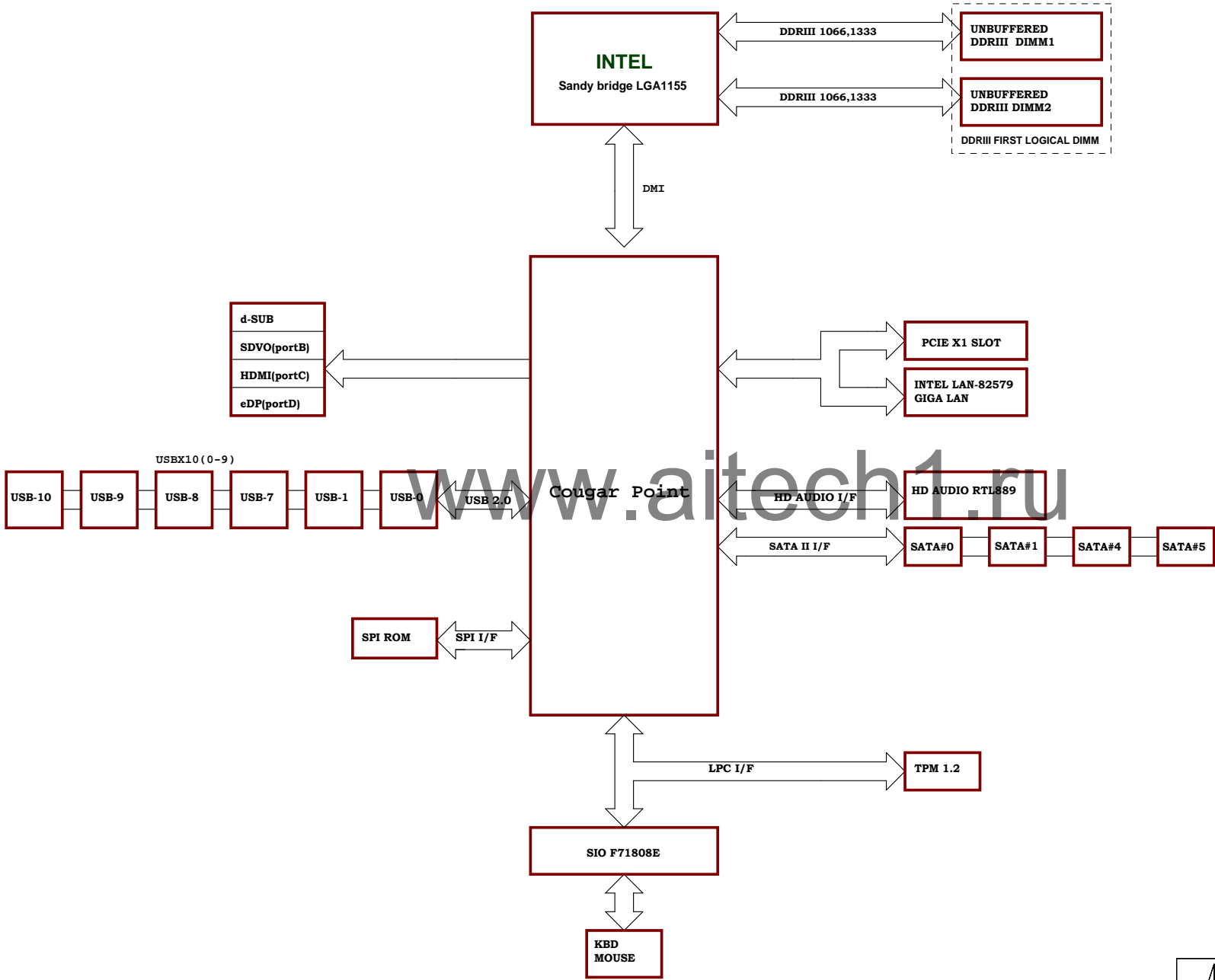
ACPI:

UPI

Other:

SATA(SATA2-300MB/s) *4

USB2.0 *6





www.aitech1.ru

PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

CPU VTT

91 110 75

R17 110K/4

R2 701K/4

CPU VTT

H_PWRGD R31 X 51/4

H_PECI R23 X 1K1%/4

H_CATERR# R341 X 1K/4

H_THERMTRIP# R33 X 51/4

H_PROCHOT# R32 X 51/4

XDP_CPU_PRODY# R35 X 51/4

CPURST# R35 X 51/4

H_PWRGD R58 1K1%/4

VCC5

R230 X 10K/4

VCC_DDR

R46 1001%/4

R45 1001%/4

C119 0.1u16V/Y/4

VCCSA VID

R294 1K1%/4

CPU_RESET#

3VSB

R33 4.7K/4

Q9 2N3904

R4 10K1%/4

11,16,32 PLTRST#

Q8 X 2N3904

H_PROCHOT#

SIO_TRIP# 16

CPU1C 3 OF 11

B11 PEG_RX_0

B12 PEG_RX_0

D12 PEG_RX_1

D11 PEG_RX#_1

C10 PEG_RX_2

C9 PEG_RX#_2

E10 PEG_RX_3

E9 PEG_RX_3

B8 PEG_RX_3

B7 PEG_RX#_4

C8 PEG_RX_5

C5 PEG_RX#_5

A5 PEG_RX_6

A6 PEG_RX#_6

E2 PEG_RX_7

E1 PEG_RX#_7

F4 PEG_RX_8

F3 PEG_RX#_8

G2 PEG_RX_8

G1 PEG_RX#_9

H3 PEG_RX_10

H4 PEG_RX#_10

J1 PEG_RX_11

J2 PEG_RX#_11

K3 PEG_RX_12

K4 PEG_RX#_12

L1 PEG_RX_13

L2 PEG_RX#_13

M3 PEG_RX_14

M4 PEG_RX#_14

N1 PEG_RX_15

N2 PEG_RX#_15

D1M_TX_0

D1M_TX#_0

D1M_TX_1

D1M_TX#_1

D1M_TX_2

D1M_TX#_2

D1M_TX_3

D1M_TX#_3

PE_TX_0

PE_TX#_0

PE_TX_1

PE_TX#_1

PE_TX_2

PE_TX#_2

PE_TX_3

PE_TX#_3

PEG_ICOMPO

PEG_COMPI

CPU1D 4 OF 11

AC8 FDI_TX0

AC7 FDI_TX0#

AC2 FDI_TX1

AC3 FDI_TX1#

AD2 FDI_TX2

AD1 FDI_TX2#

AD4 FDI_TX3

AD3 FDI_TX3#

AD7 FDI_TX4

AD6 FDI_TX4#

AE7 FDI_TX5

AE8 FDI_TX5#

AE3 FDI_TX6

AE2 FDI_TX6#

AG2 FDI_TX7

AG1 FDI_TX7#

FDI_TX0

FDI_TX#_0

FDI_TX_1

FDI_TX#_1

FDI_TX_2

FDI_TX#_2

FDI_TX_3

FDI_TX#_3

FDI_TX_4

FDI_TX#_4

FDI_TX_5

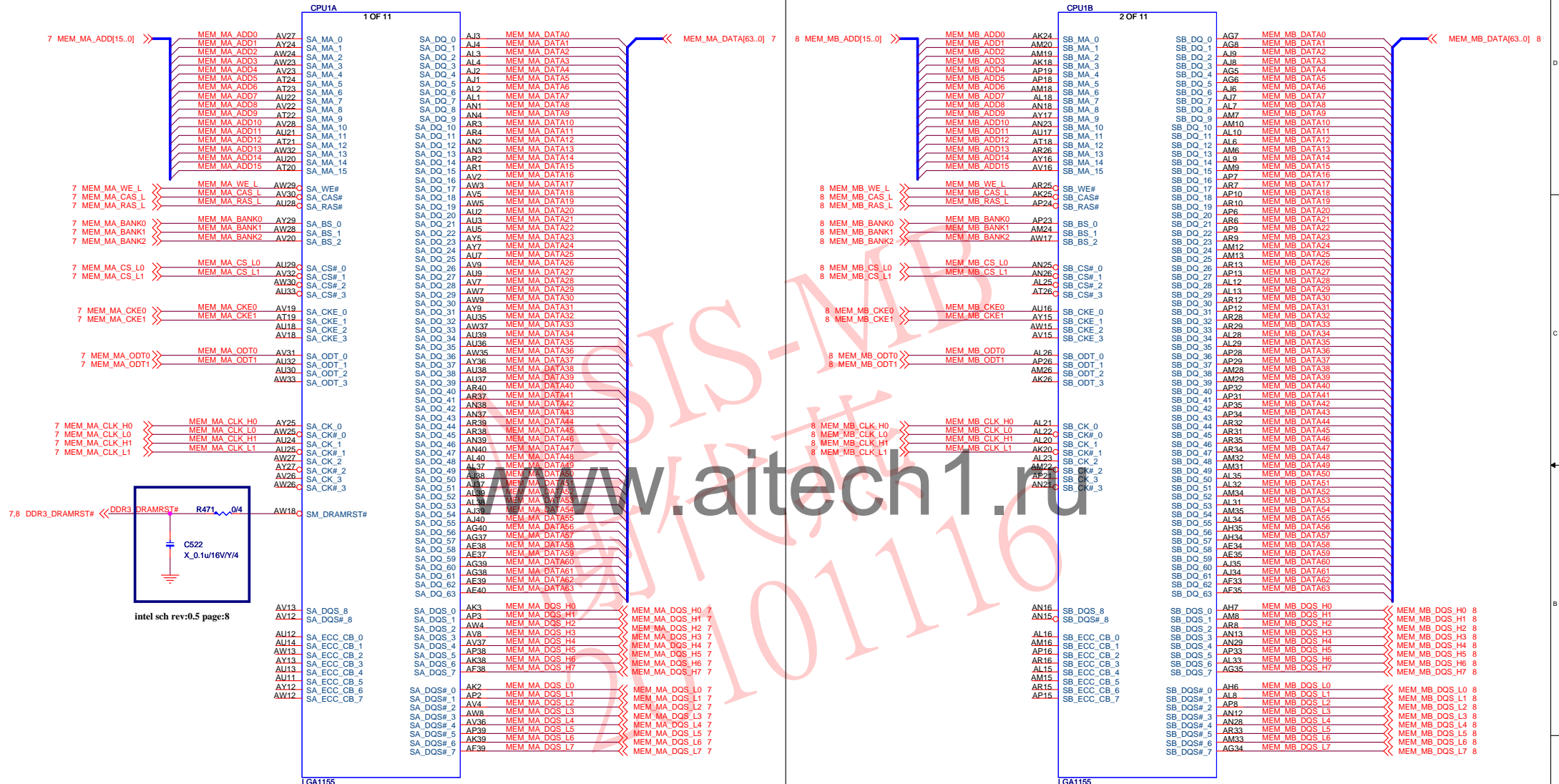
FDI_TX#_5

FDI_TX_6

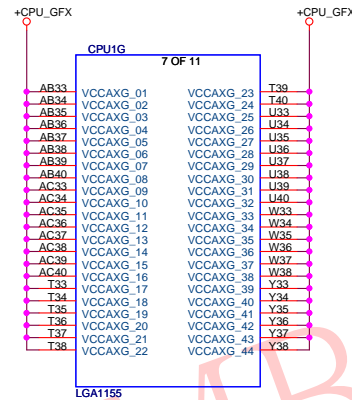
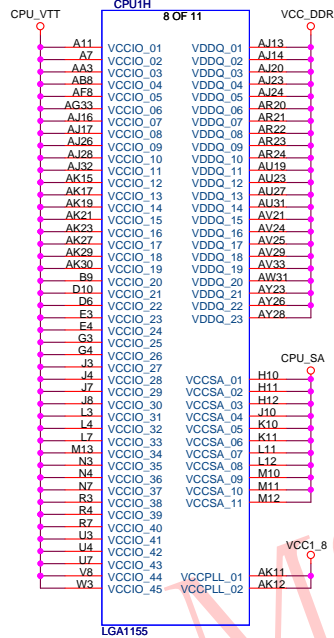
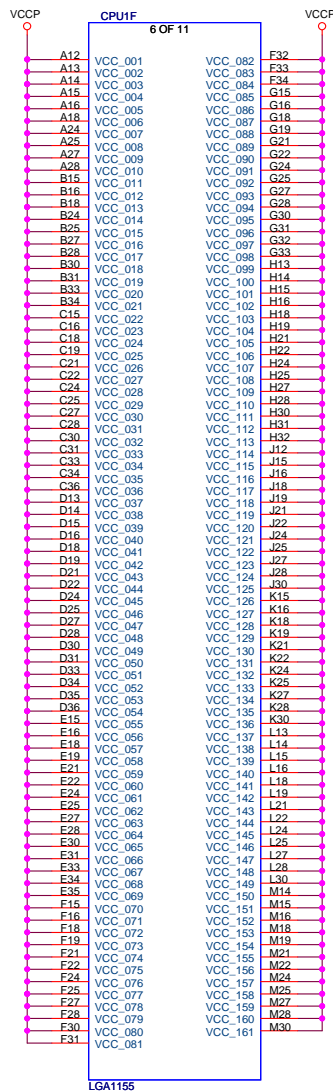
FDI_TX#_6

FDI_TX_7

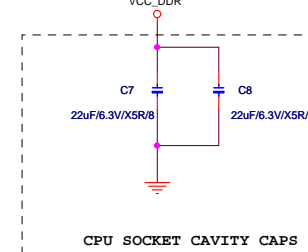
FDI_TX#_7



intel sch rev:0.5 page:8

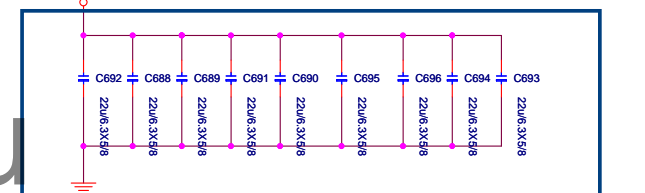
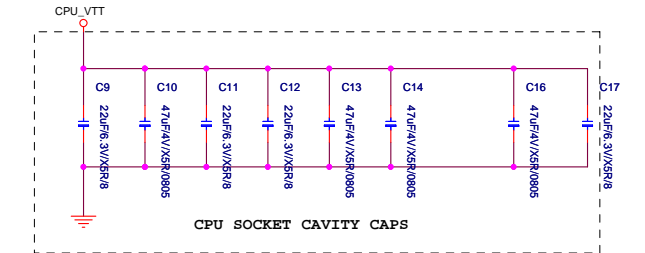
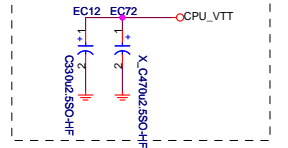


+1.5V_DDR3-Decoupling

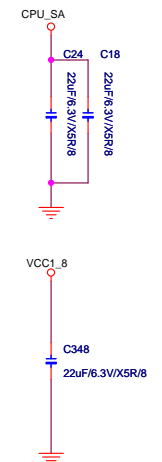
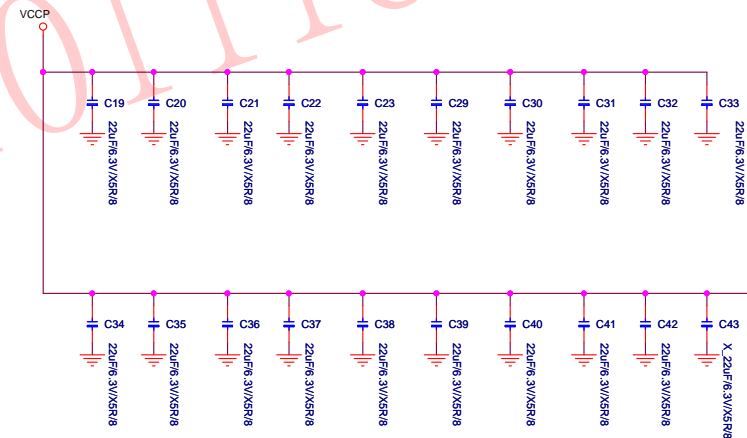


+CPU_VTT Decoupling

button SP Capacitors



+CPU_VCCP-Decoupling



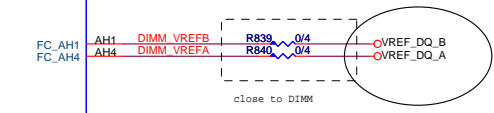
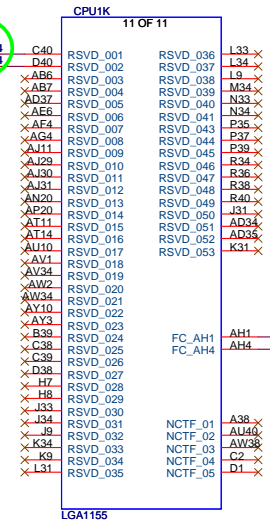
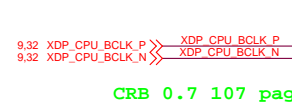
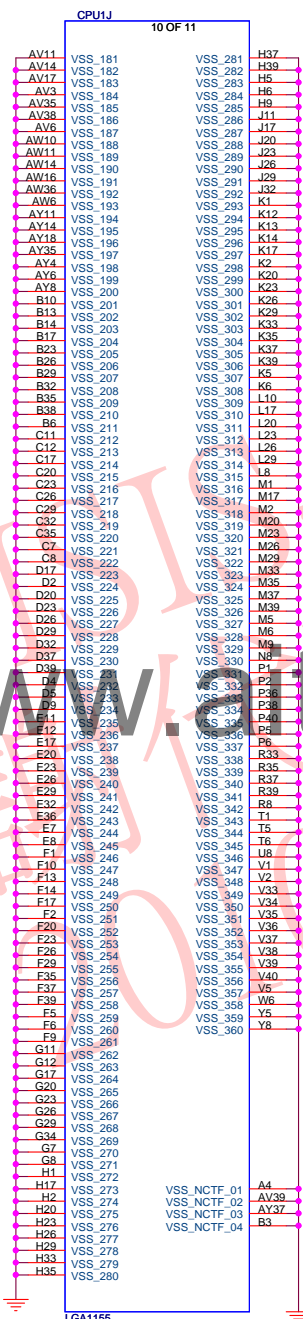
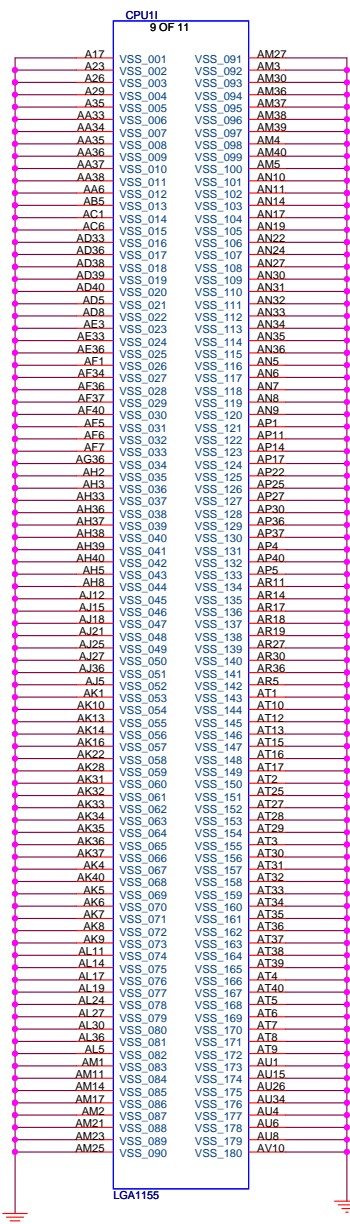
PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY



MICRO-STAR INT'L CO.,LTD

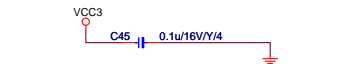
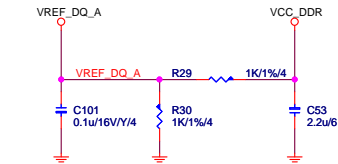
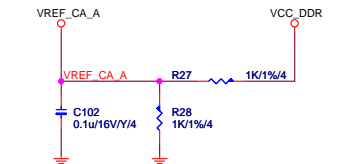
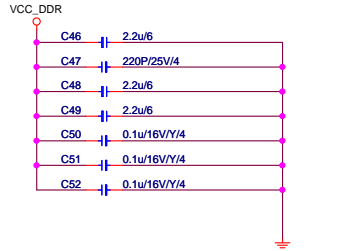
MS-7677

Size	Document Description	Rev
Custom	CPU-Power	1.0
Date: Tuesday, November 16, 2010	Sheet 5 of 33	

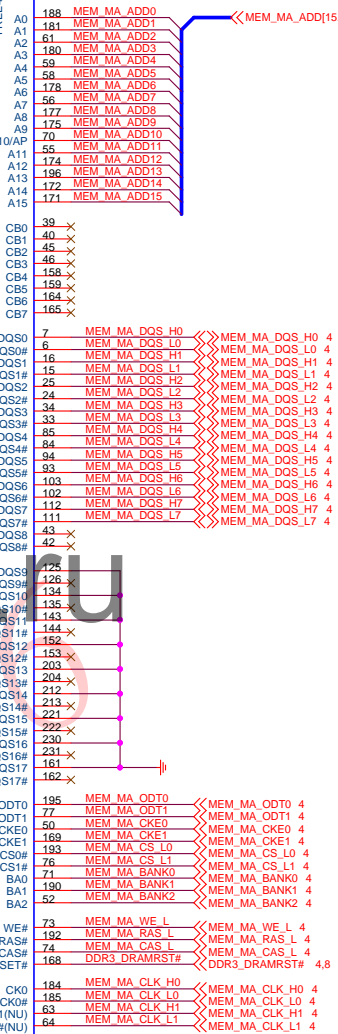


DDRIII DIMM_A0


Place close to DIMM1



4 MEM_MA_DATA[63..0] <<> MEM_MA_DATA[63..0]

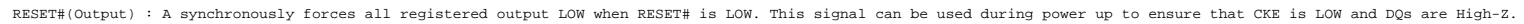
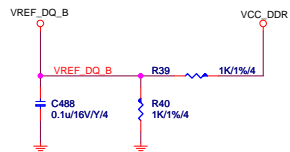



DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

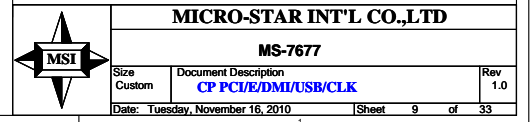


MICRO-STAR INT'L CO.,LTD		
MS-7677		
Size	Document Description	Rev
Custom	DDR III A DIMM 1	1.0
Date: Tuesday, November 16, 2010		Sheet 7 of 33

DDR3



	MICRO-STAR INT'L CO.,LTD		
	MS-7677		
	Size Custom	Document Description DDR III B DIMM 1	Rev 1.0
	Date: Tuesday, November 16, 2010		Sheet 8 of 33



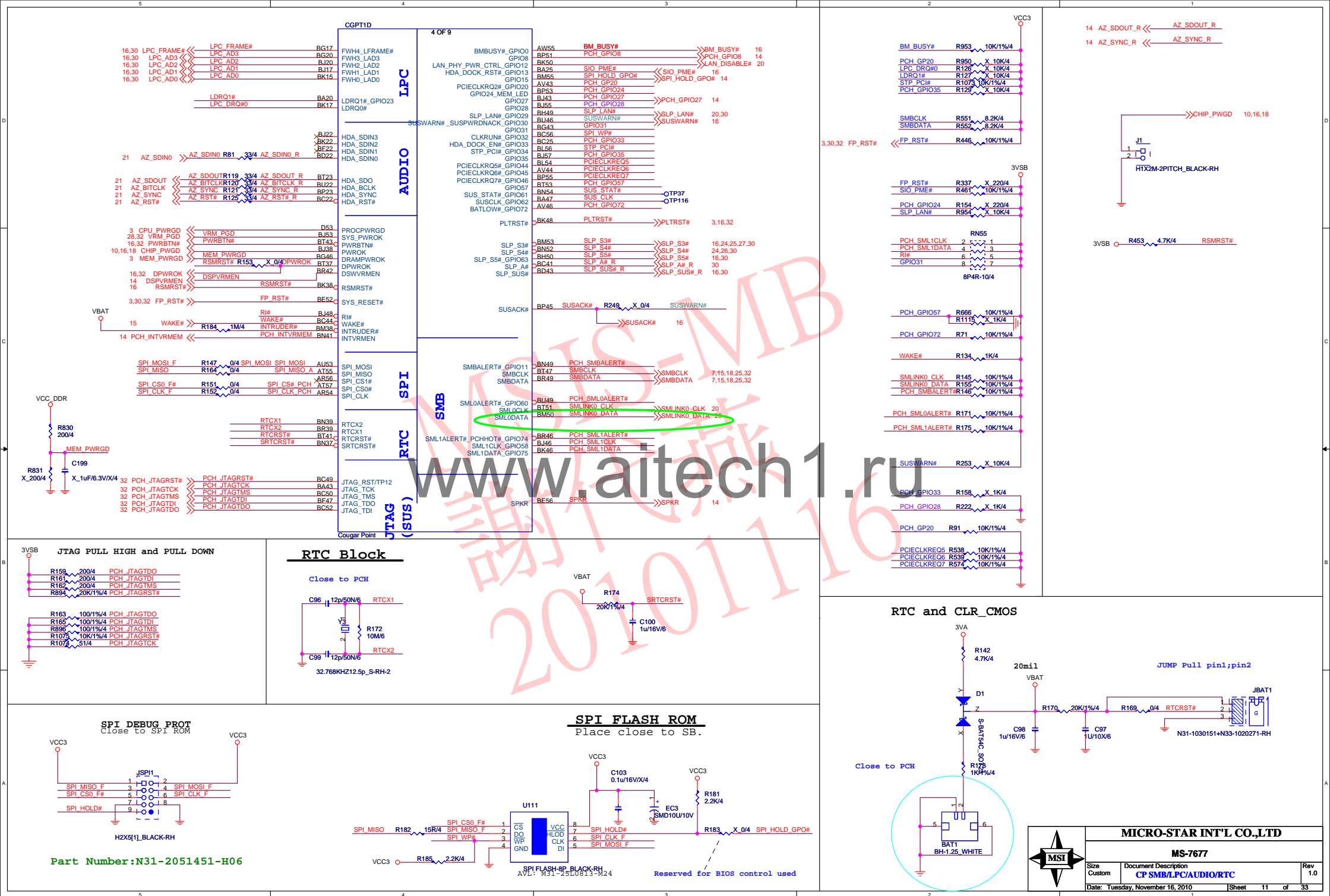
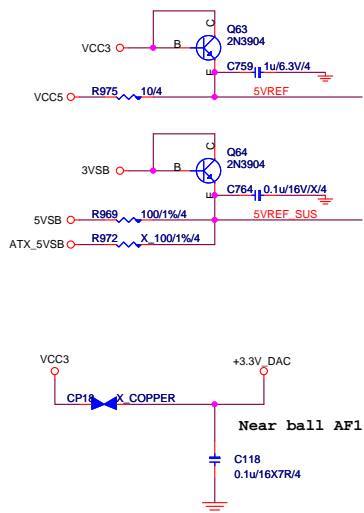


Table 3-7. VCCPLL Decoupling Requirements

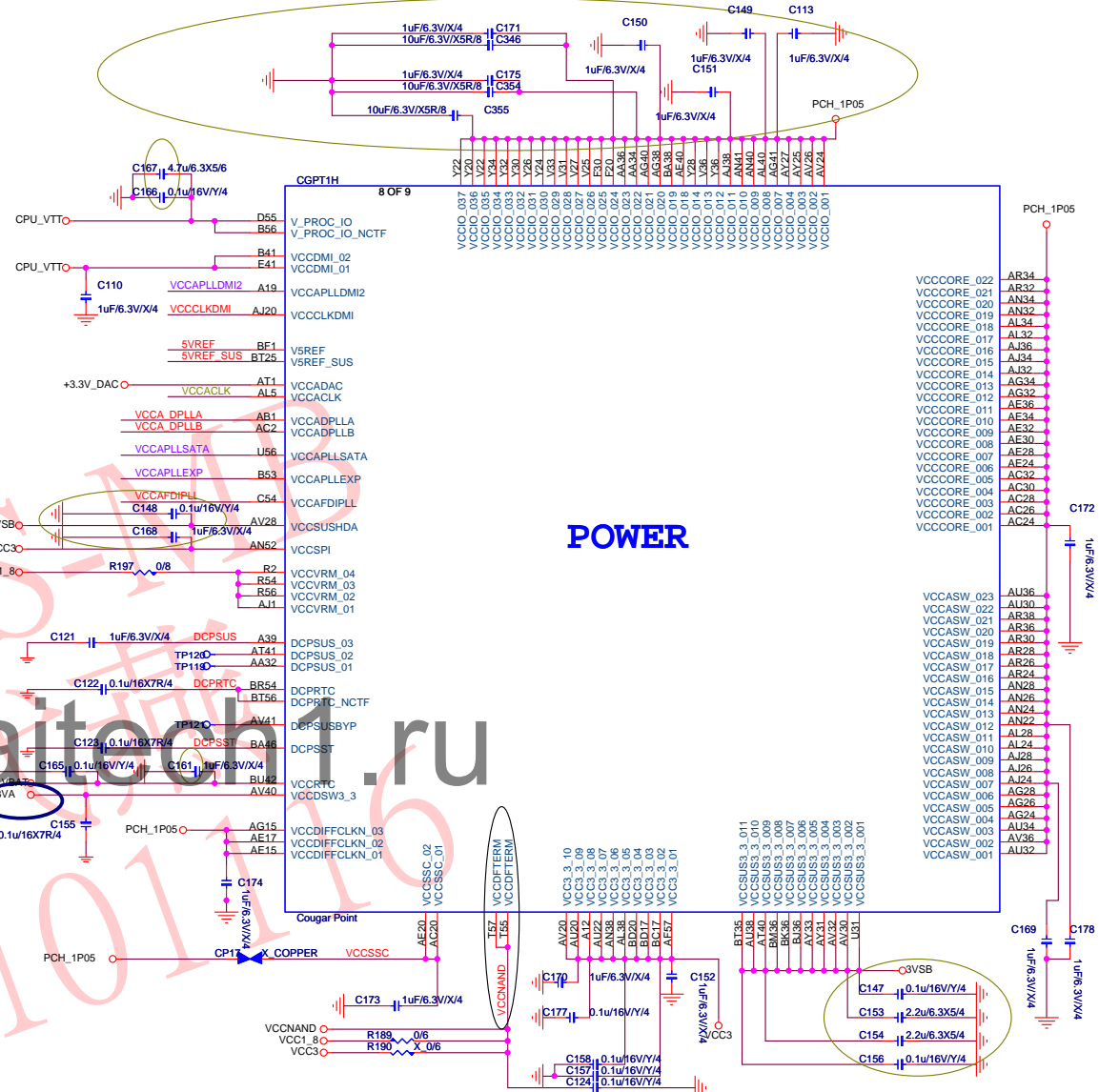
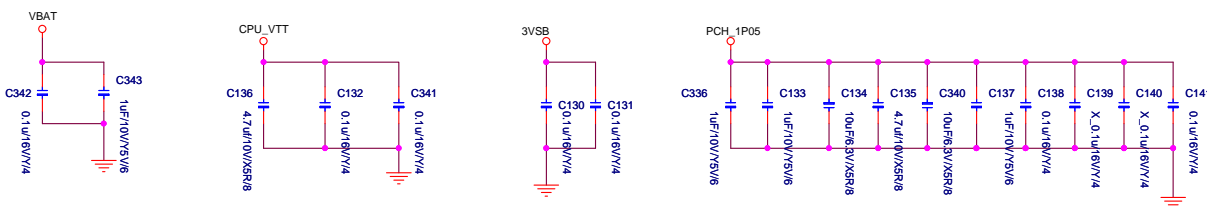
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µF 0805 XSR	1	3mΩ	0.51nH	Output		1, 2, 3

5VREF & 5VREF_SUS Sequencing Circuit



Near ball AF1

PCH decoupling cap



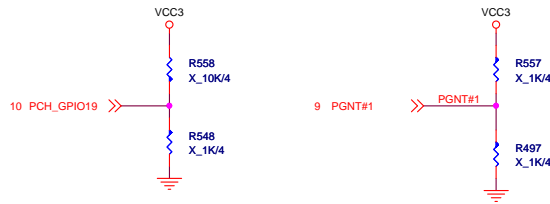
MICRO-STAR INT'L CO.,LTD

MS-7677

Size Custom	Document Description CP POWER	Rev 1.0
Date: Tuesday, November 16, 2010		Sheet 12 of 33

CP REQUIRED STRAPS

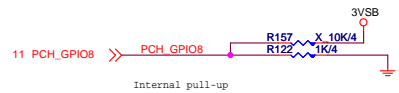
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



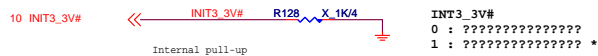
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

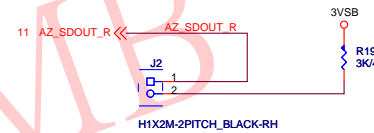


DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.



HDA_SYNC
0D PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

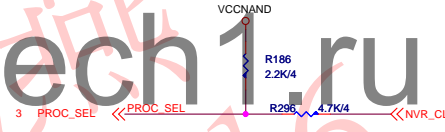


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

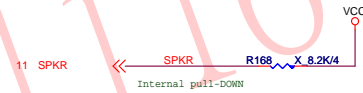
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



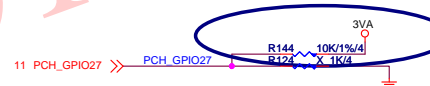
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



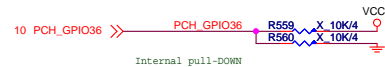
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



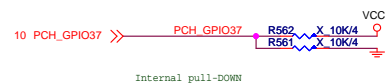
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up (8.2k-10k) to VccDSW3_3



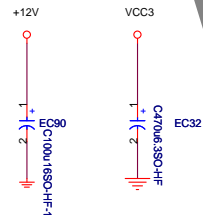
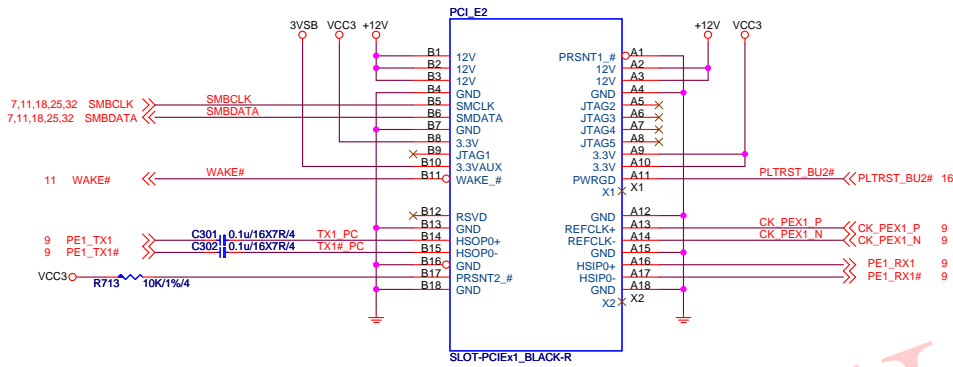
Cougar point EDS PAGE:93 This signal should not be pull high



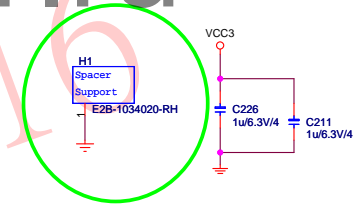
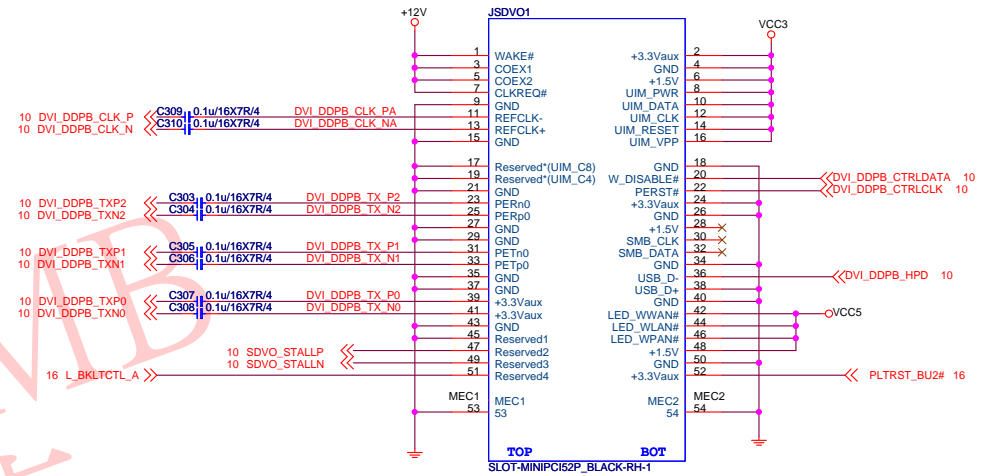
Cougar point EDS PAGE:93 This signal should not be pull high

	MICRO-STAR INT'L CO.,LTD		
	MS-7677		
	Size Custom	Document Description CP STRAPS	Rev 1.0
	Date: Tuesday, November 16, 2010	Sheet 14 of 33	

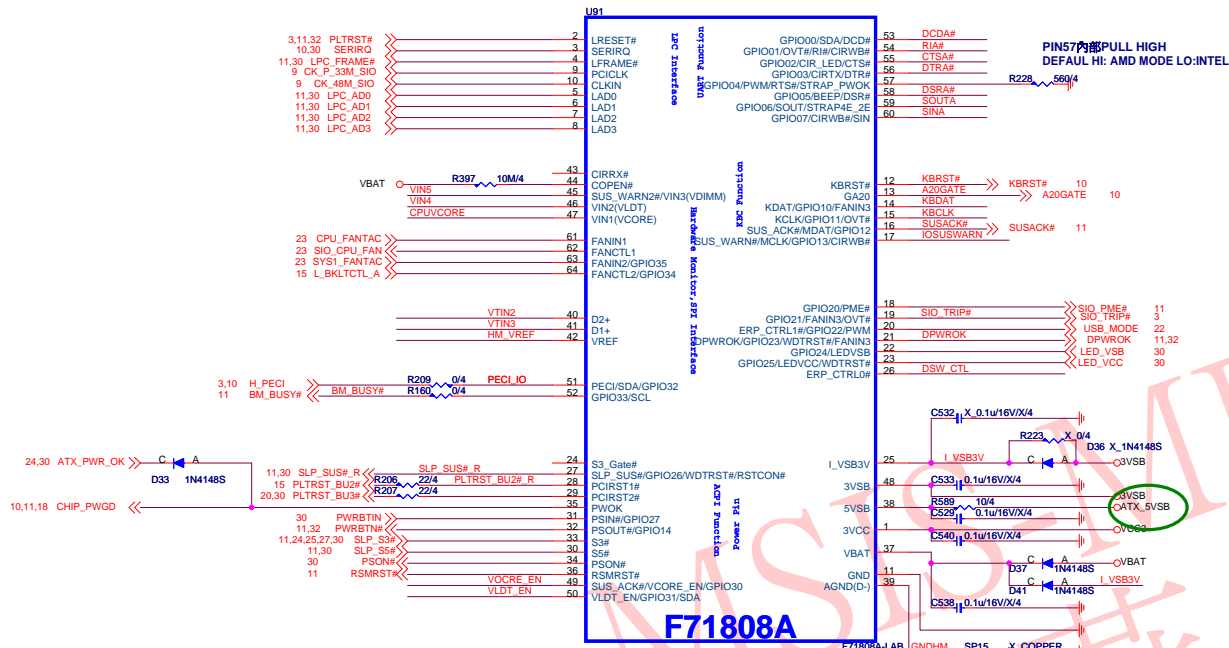
PCI EXPRESS x1-PORT1



SDVO connect

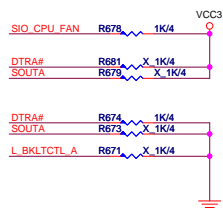


www.aitech1.ru

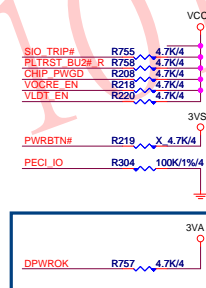


LPC I/O STRAPPING RESISTOR

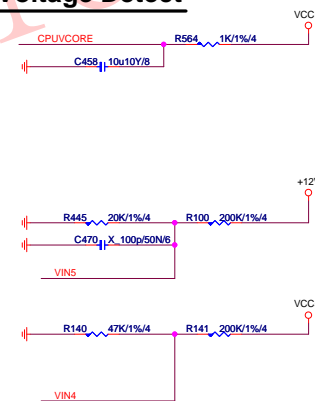
POWER-ON TRIP



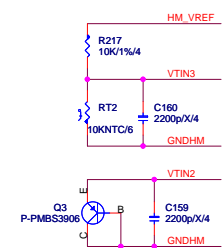
PIN	Function	NET Name	HI	LO
64	L_BKLTCTL_A	FANCTL2	PWM FAN	LINEAR FAN
62	SIO_CPU_FAN	FANCTL1	PWM FAN	not support linear fan
56	DTRA#	FAN40_100	FAN SPEED DUTY:40%	FAN SPEED DUTY:100%
59	STRAP4E_2E	Config 4E/2E	4E(DEFAULT)	2E
57	STRAP_PWOK	STRAP_PWOK	AMD (DEFAULT)	INTEL



Voltage Detect



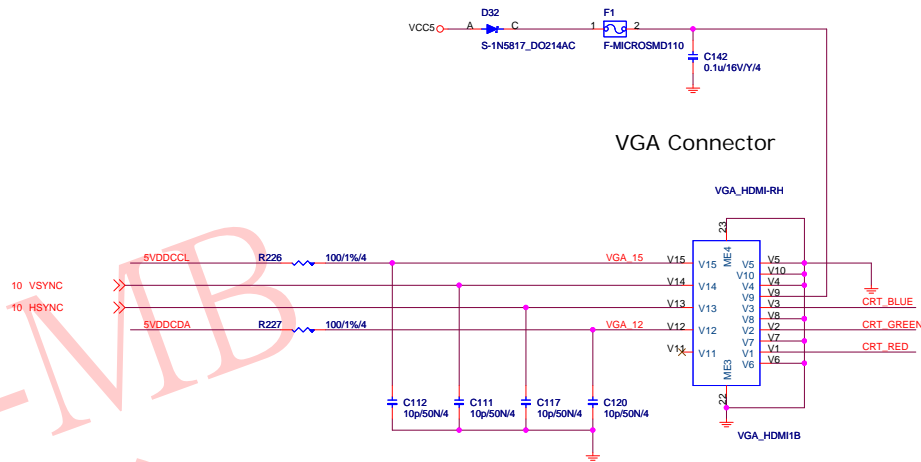
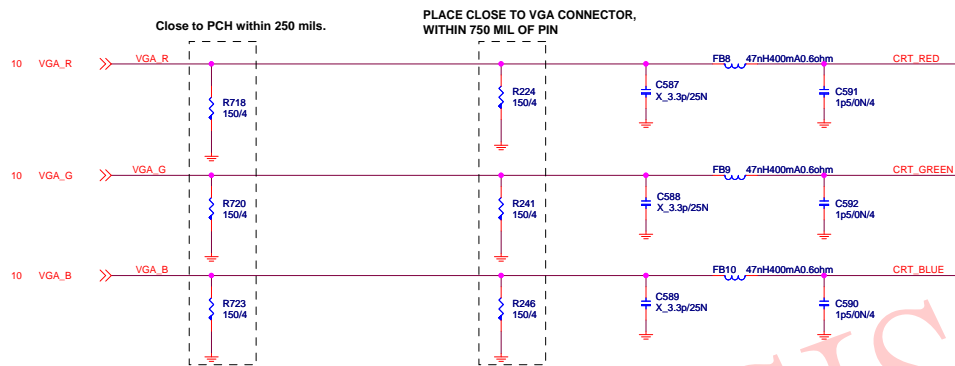
Thermal Resistor



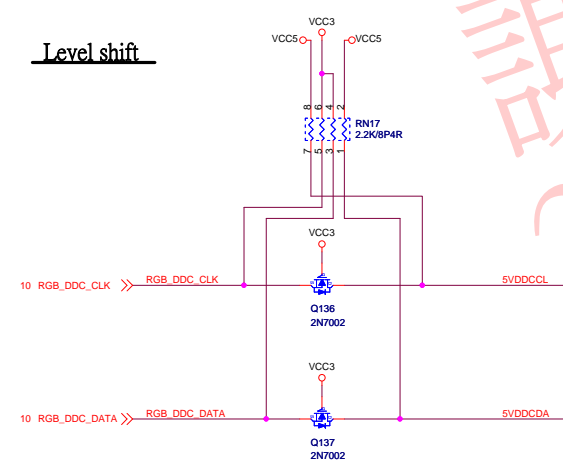
MICRO-STAR INT'L CO.,LTD

MS-7677

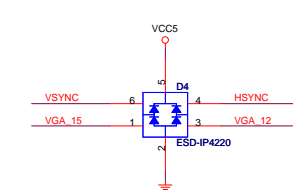
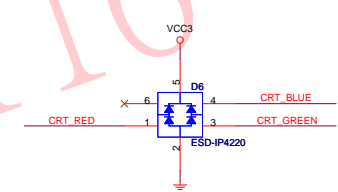
Size	Document Description	Rev
Custom	SIO-Fintek F71808E	1.0
Date: Tuesday, November 16, 2010	Sheet 16 of 33	



Level shift

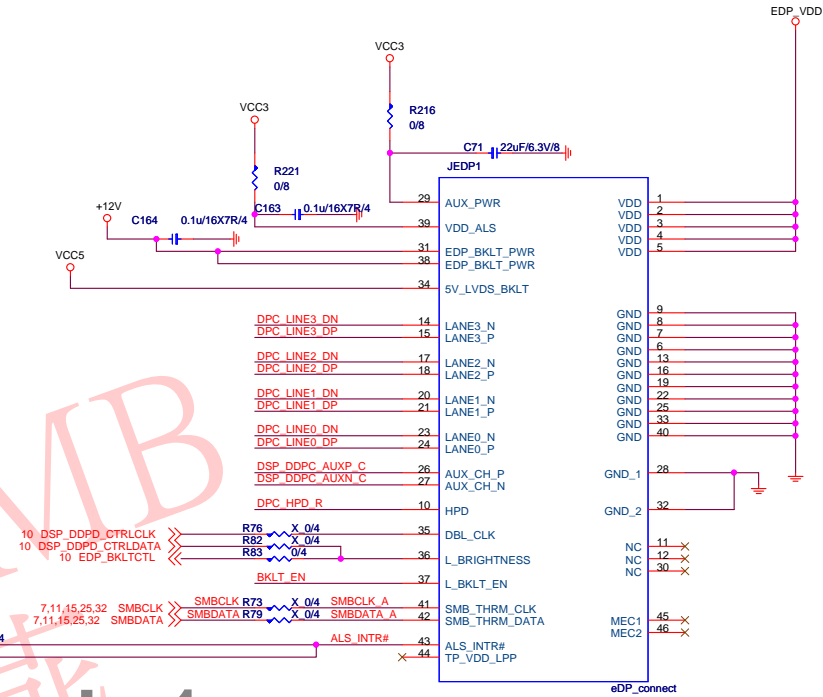
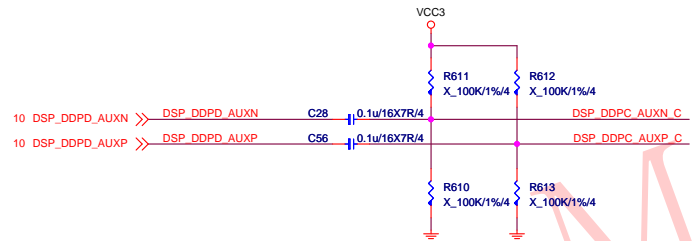
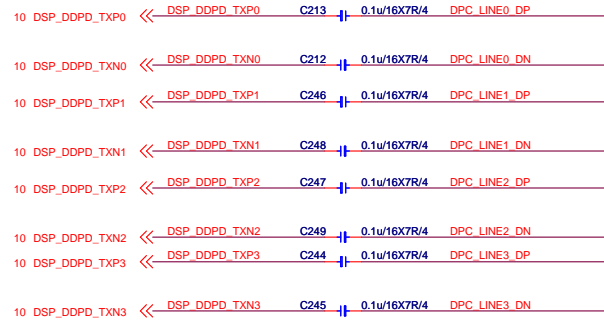


For EMI

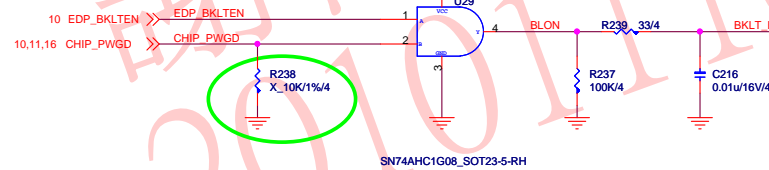
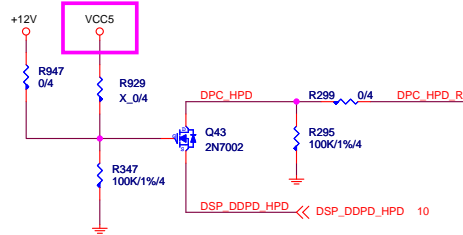


www.aitech1.ru

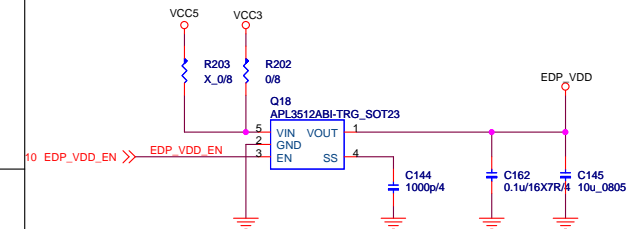
MICRO-STAR INT'L CO.,LTD			
MS-7677			
Size	Document Description	Rev	
Custom	VGA	1.0	
Date: Tuesday, November 16, 2010		Sheet	17 of 33



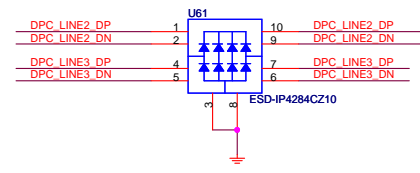
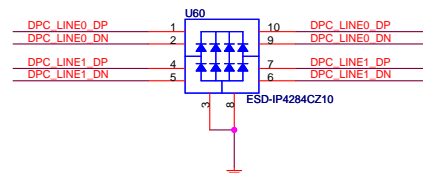
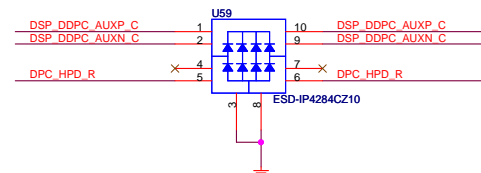
www.aitech1.ru



EDP POWER

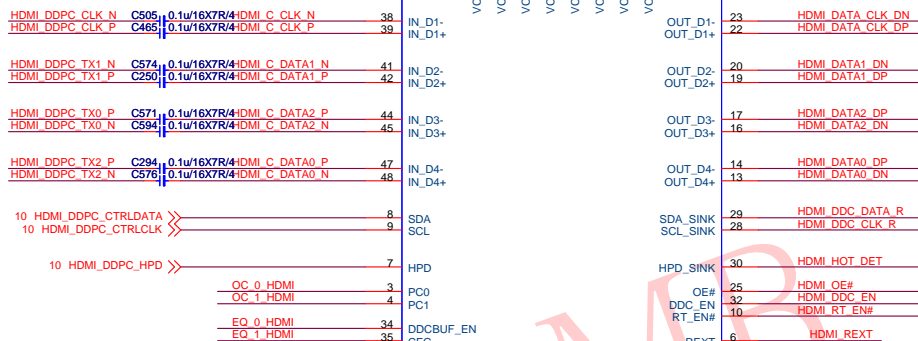
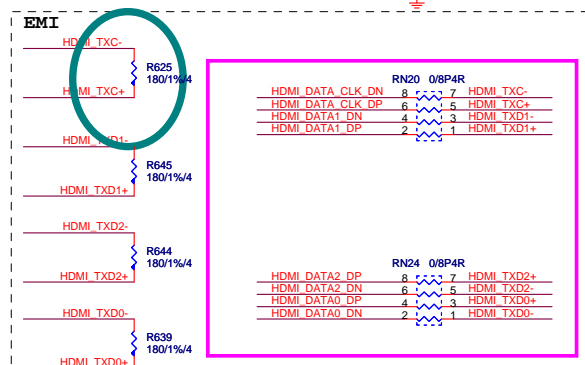
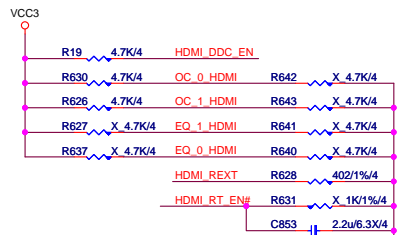


For EMI



HDMI level shifter

10 HDMI_DDPCLK_P <=> HDMI_DDPCLK_P
10 HDMI_DDPCLK_N <=> HDMI_DDPCLK_N
10 HDMI_DDPCLK_TX2_P <=> HDMI_DDPCLK_TX2_P
10 HDMI_DDPCLK_TX2_N <=> HDMI_DDPCLK_TX2_N
10 HDMI_DDPCLK_TX1_P <=> HDMI_DDPCLK_TX1_P
10 HDMI_DDPCLK_TX1_N <=> HDMI_DDPCLK_TX1_N
10 HDMI_DDPCLK_TX0_P <=> HDMI_DDPCLK_TX0_P
10 HDMI_DDPCLK_TX0_N <=> HDMI_DDPCLK_TX0_N



PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.

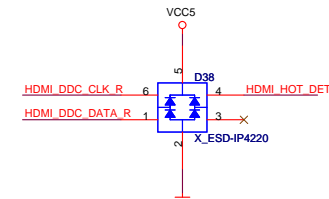
www.aitech1.ru

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

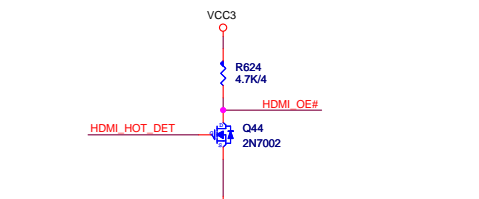
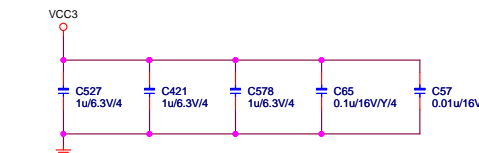
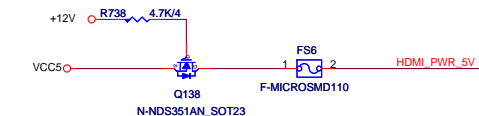
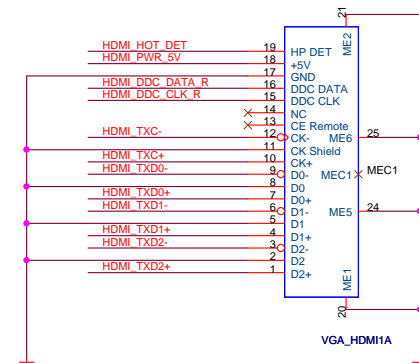
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

reserve



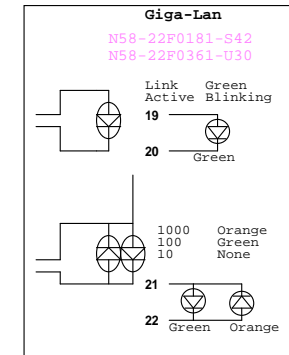
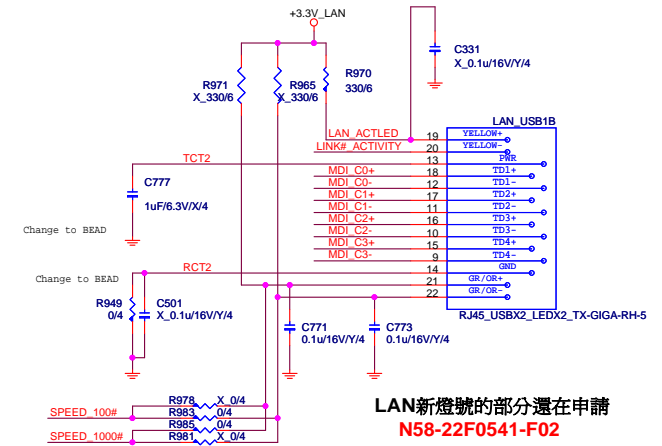
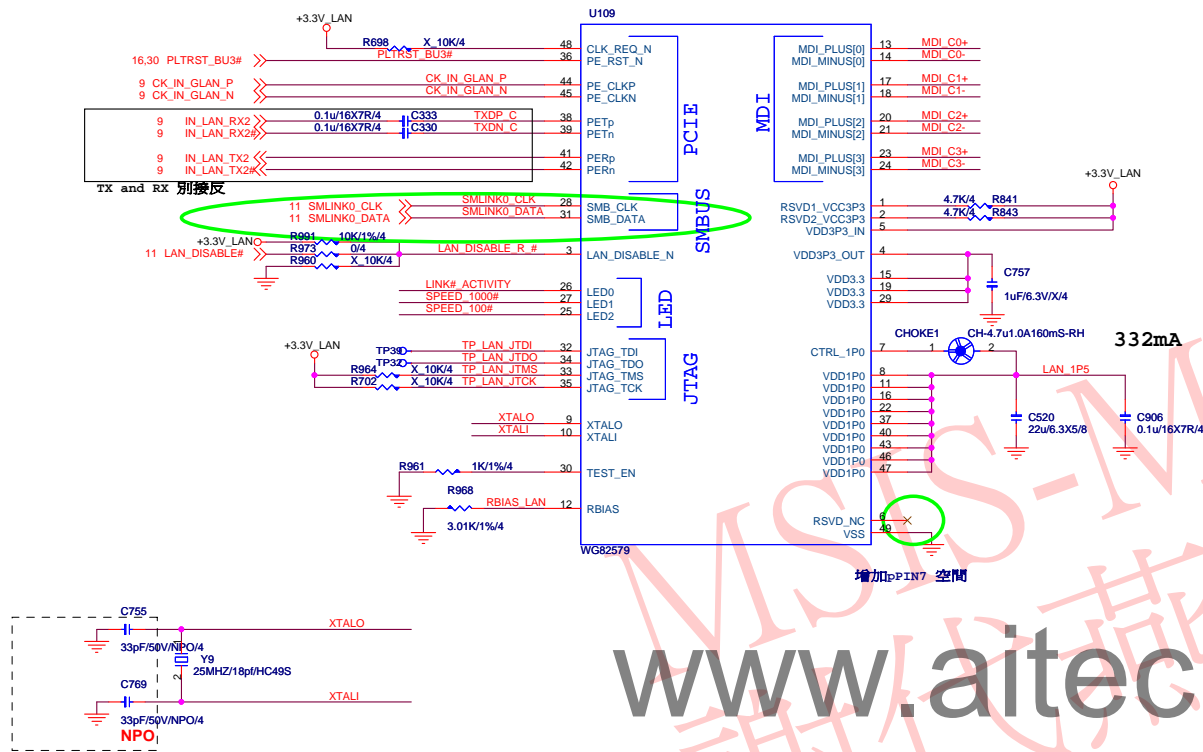
VGA_HDMI-RH



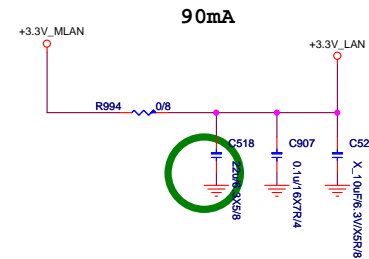
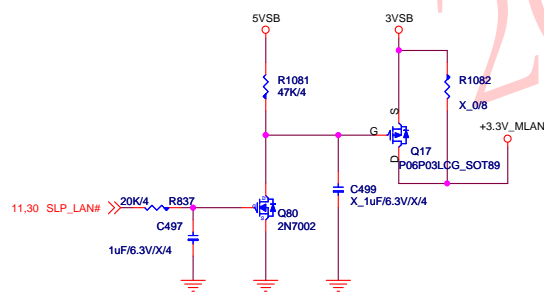
MICRO-STAR INT'L CO.,LTD			
MS-7677			
Size	Document Description	Rev	
Custom	HDMI	1.0	
Date: Tuesday, November 16, 2010	Sheet	19	of 33

$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,
the CLK_REQ_N pull-up resistor should be connected
to +V3.3s



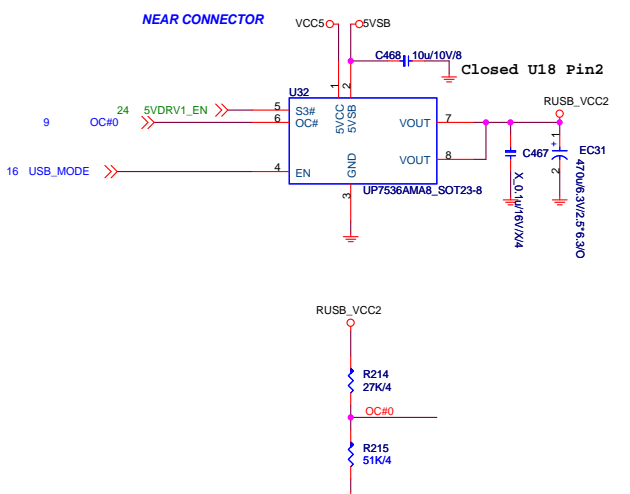
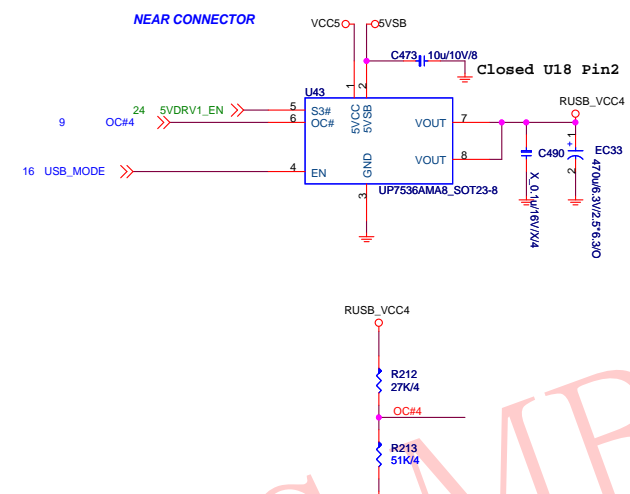
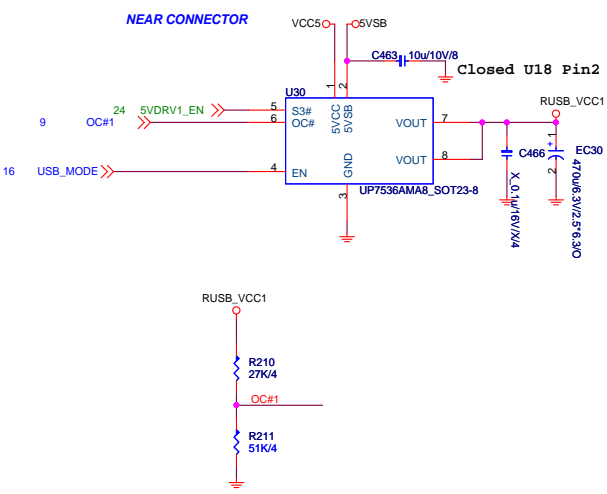
+3.3V LAN



Note: These caps closed to PHY

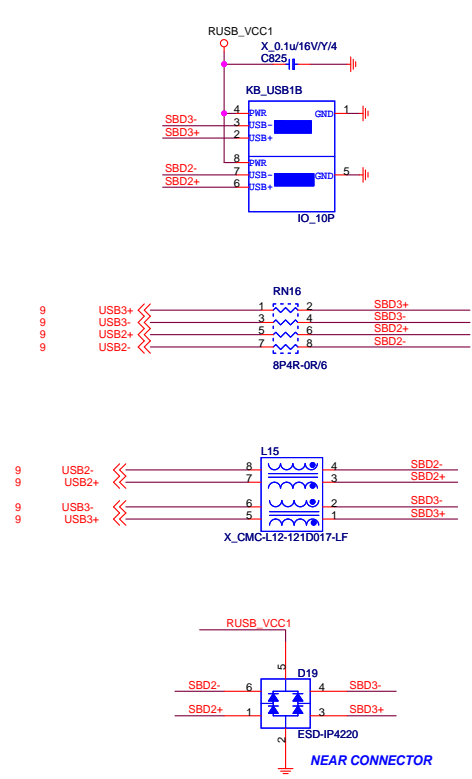
Rear USB Connector

USB POWER FOR PORT

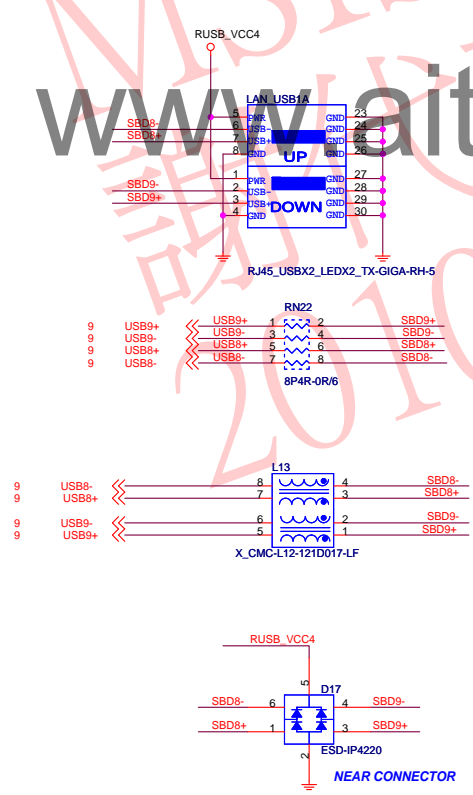


REAR USB

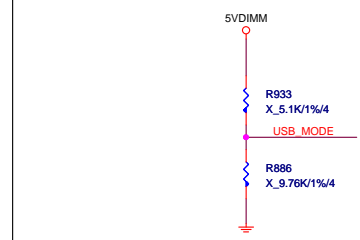
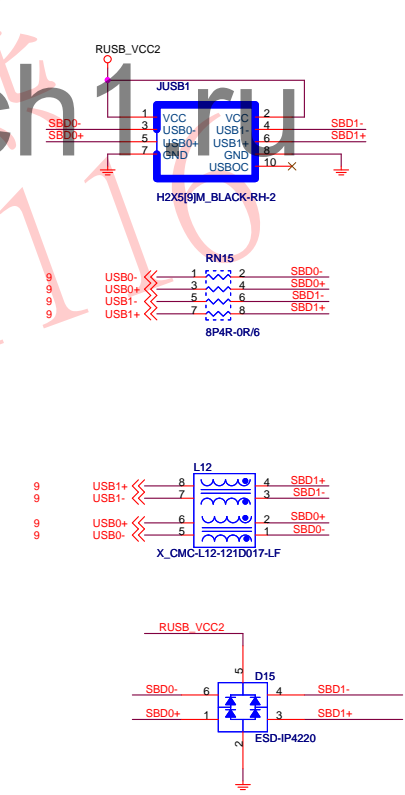
PS2&USBX2 PORT(6,7)

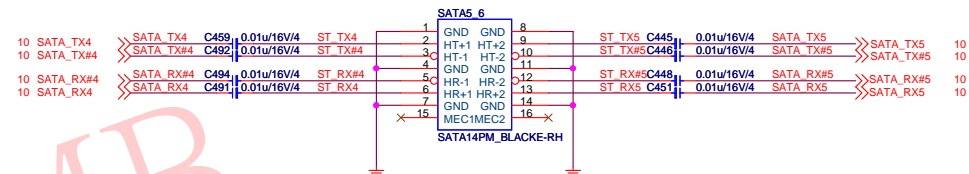


REAR USB PORT 8,9 (With LAN)

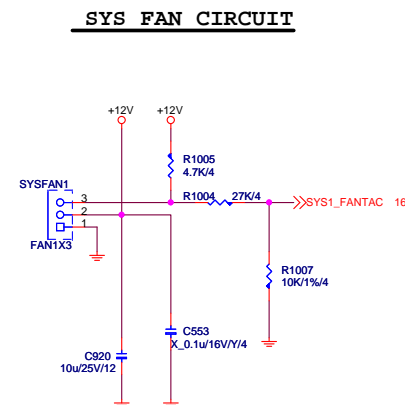


REAL USB PORT 0,1





www.aitech1.ru

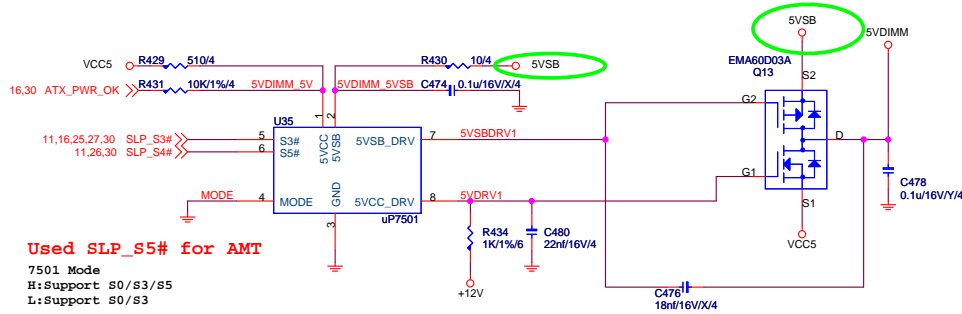


MICRO-STAR INT'L CO.,LTD

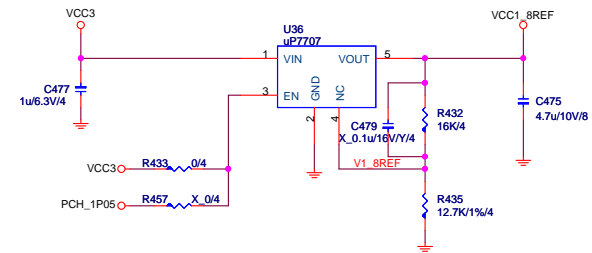
MS-7677

Size Custom	Document Description SATA /FAN Control	Rev 1.0
Date: Tuesday, November 16, 2010		Sheet 23 of 33

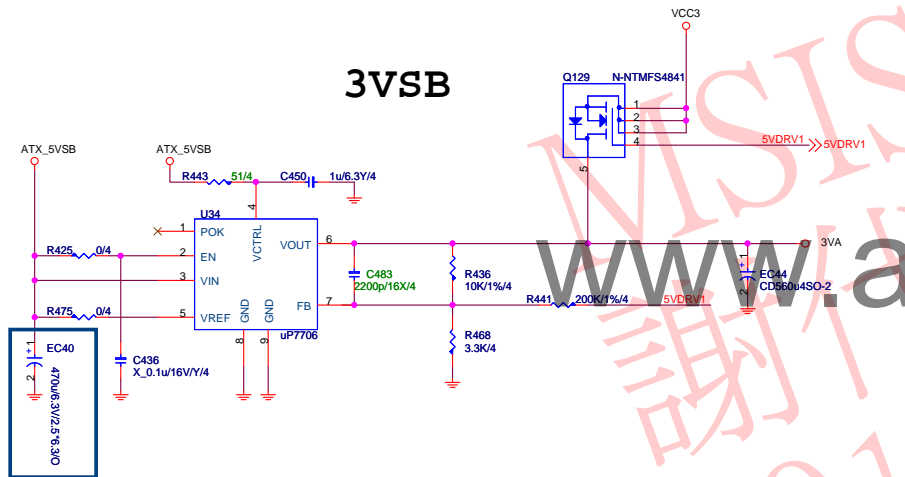
5VDIMM FOR DDR



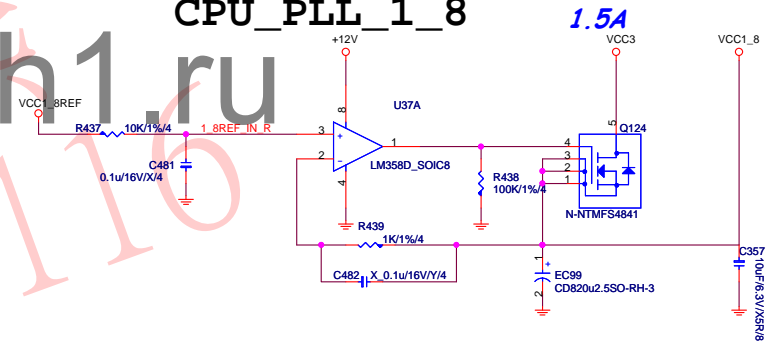
VCC1_8REF



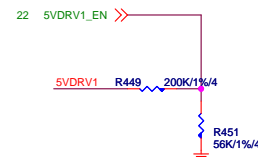
3VSB



CPU_PLL_1_8



USB MODE



MICRO-STAR INT'L CO.,LTD

MS-7677

Size	Document Description	Rev
Custom	ACPI Controller UPI	1.0
Date: Tuesday, November 16, 2010	Sheet 24 of 33	

CPU SA Power

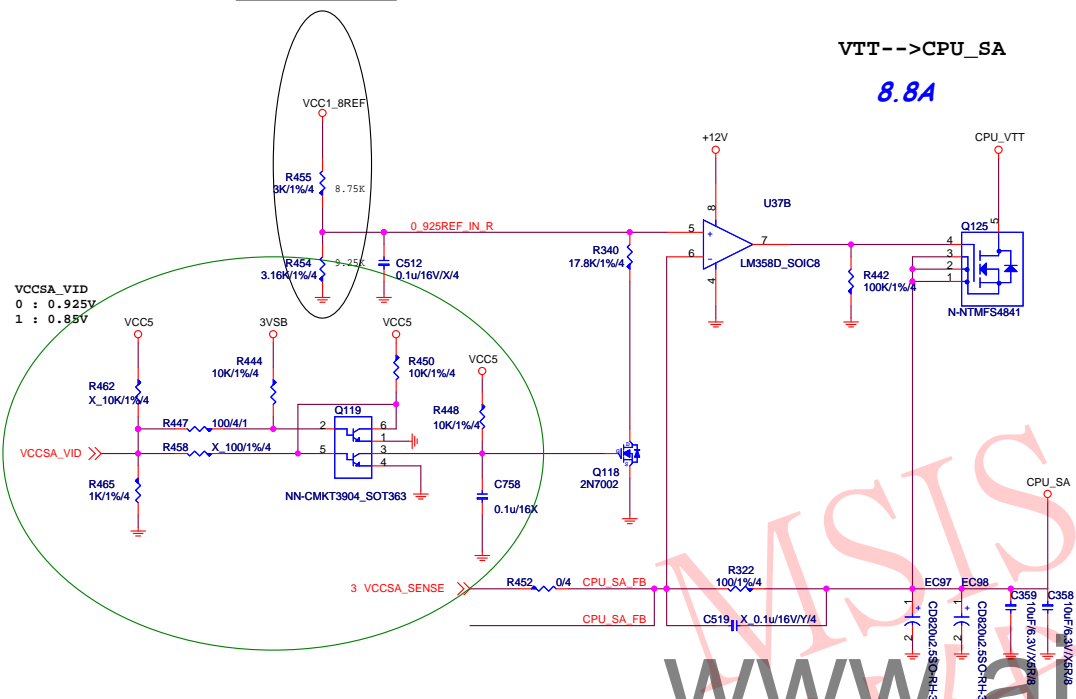
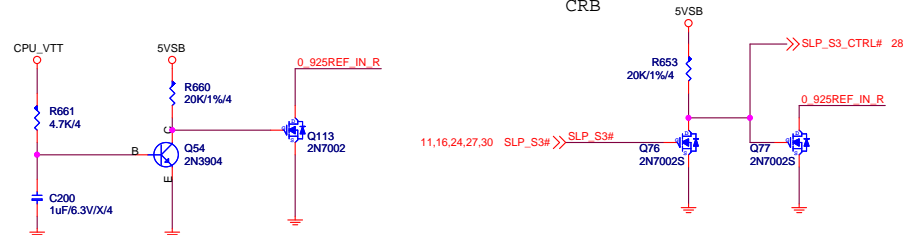


Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 WSR	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1,23

Waitting CPU_VTT Ready



CP Power

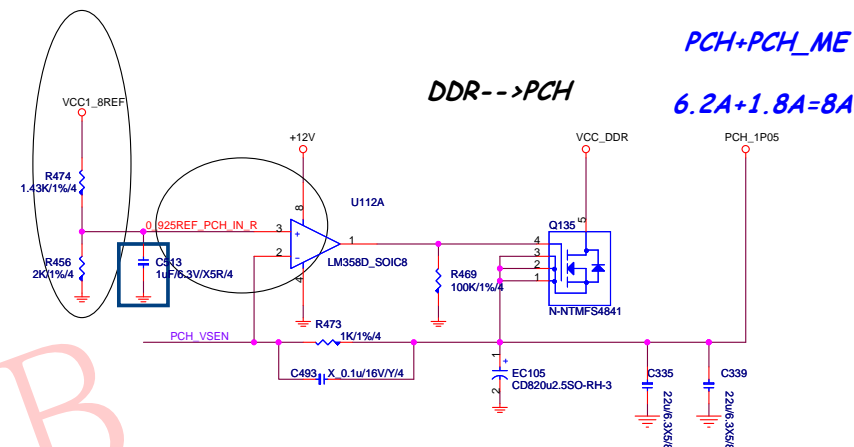
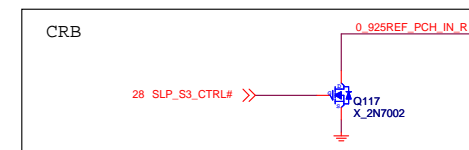
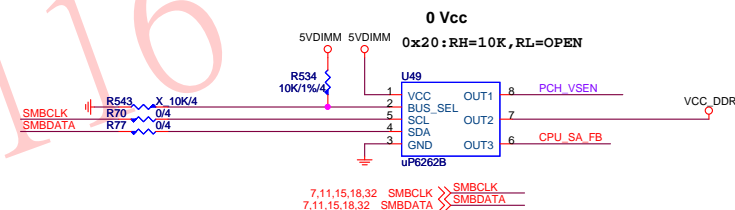


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x μF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1x560uF 3x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different than those shown.

UPI VOLTAGE CONSOLE

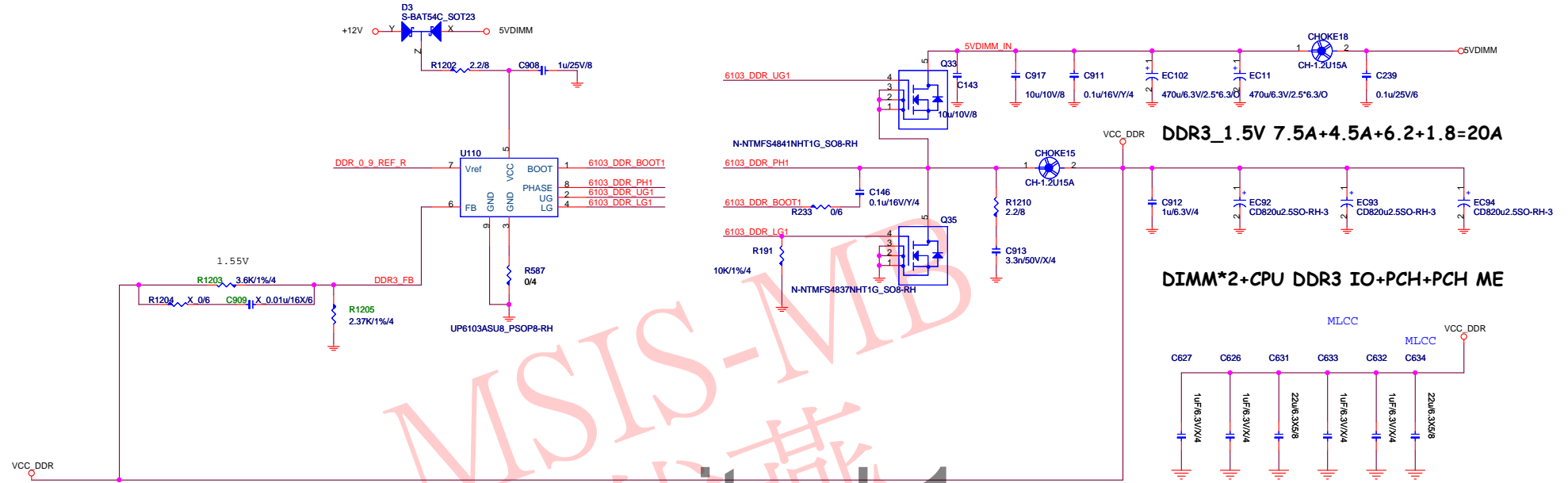


MICRO-STAR INT'L CO.,LTD

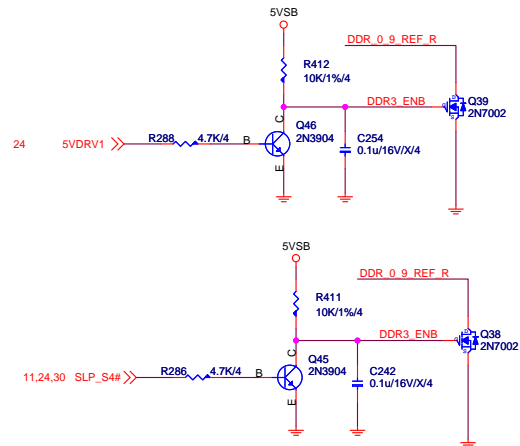
MS-7677

Size Custom	Document Description CP /CPU_SA POWER	Rev 1.0
Date: Tuesday, November 16, 2010		Sheet 25 of 33

DDR Power



Intel Power on for 5v droop issue

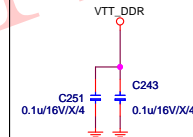


Meet Intel Power Down Sequence

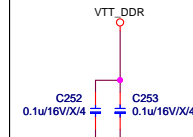
Table 3-11. VDDQ Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 1000µF	3	5mΩ	1.8nH	Output	Close to power pins	1, 2
22µF 0805 X5R	9	5mΩ	0.55nH	Output		

ChannelA DDR VTT Power CAP



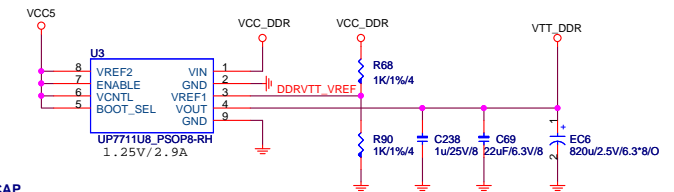
ChannelB DDR VTT Power CAP



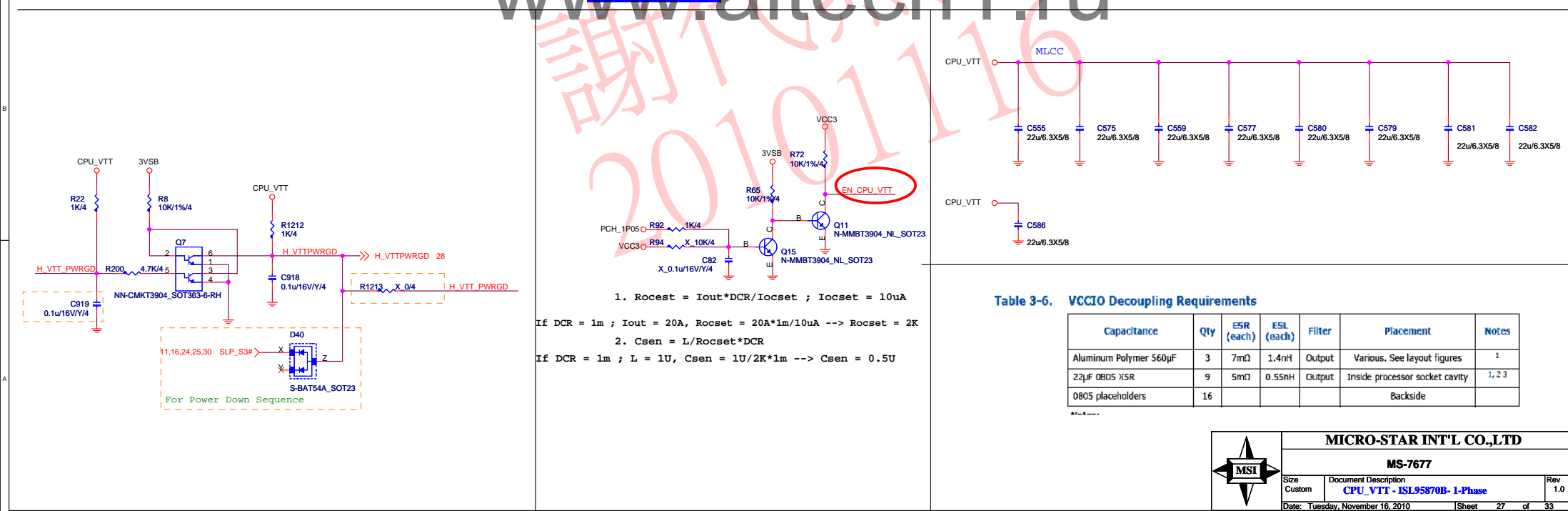
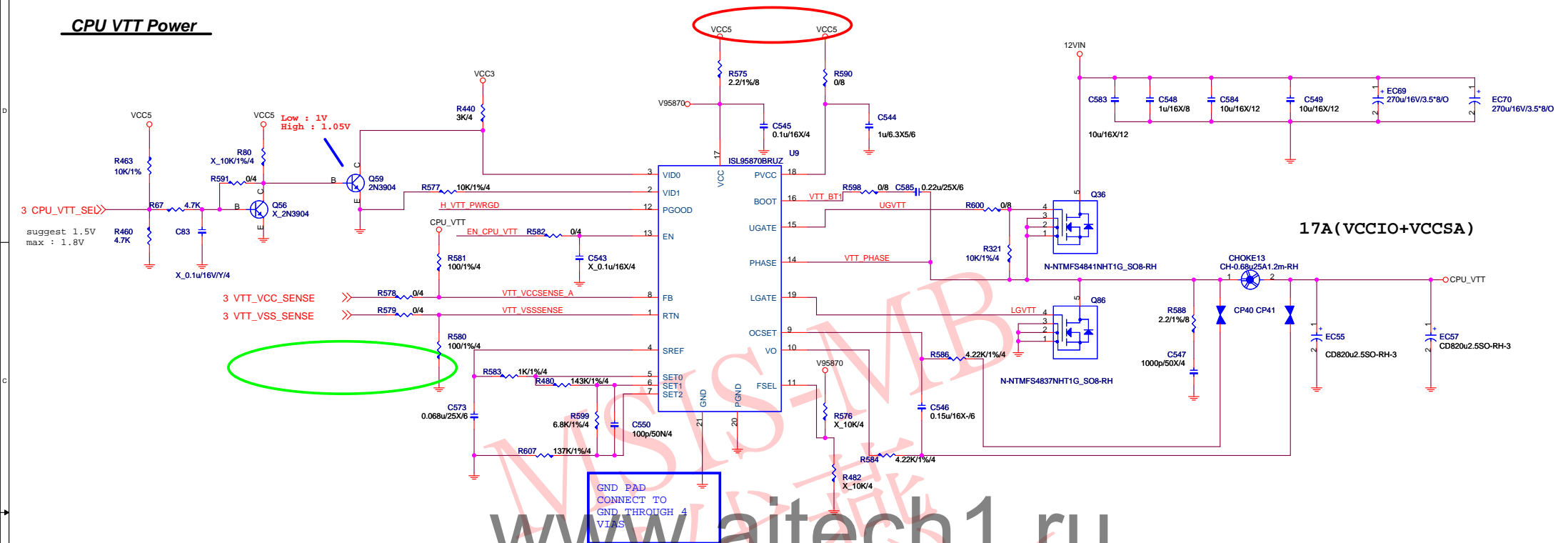
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A



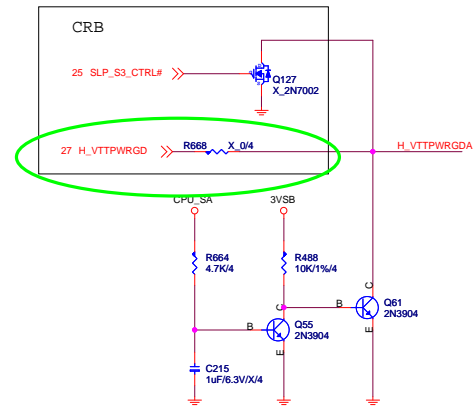
CPU VTT Power



MICRO-STAR INT'L CO.,LTD

MS-7677

Size	Document Description	Rev
Custom	CPU_VTT - ISL95870B- 1-Phase	1.0
Date:	Tuesday, November 16, 2010	Sheet 27 of 33

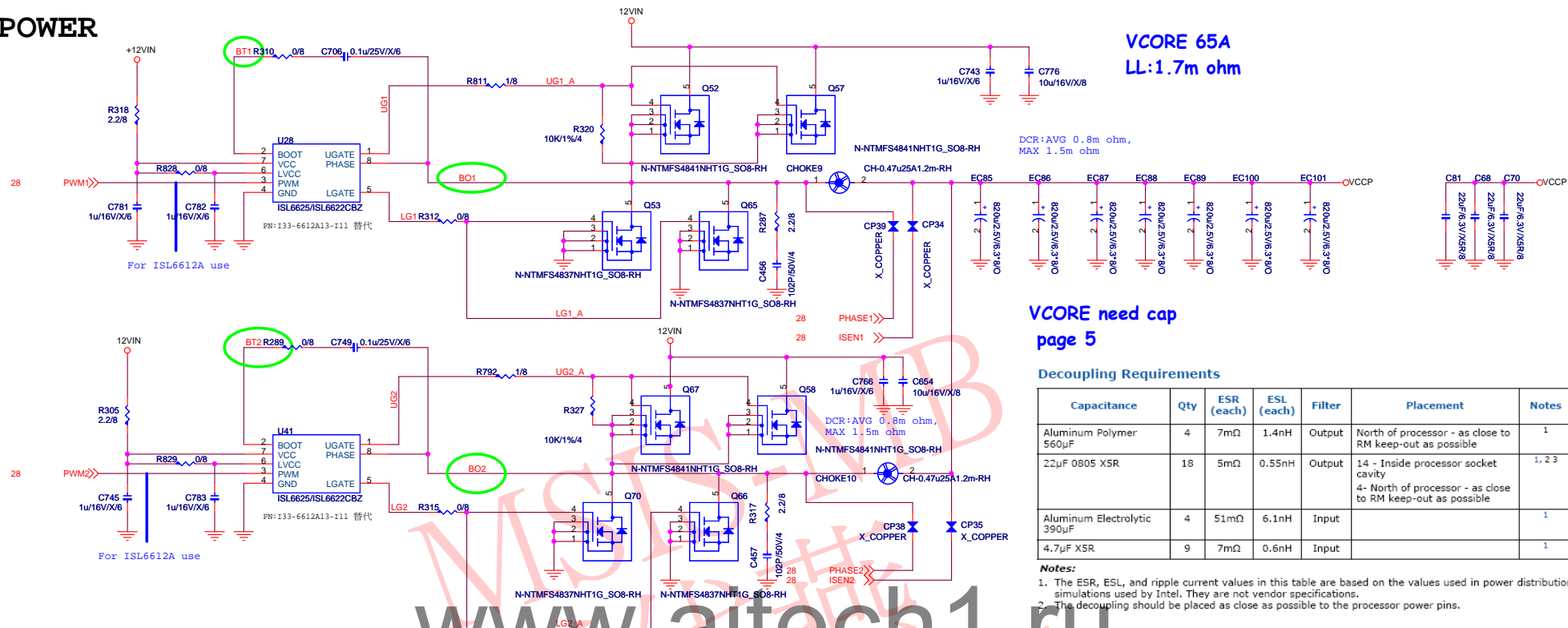
[illegible]

The schematic diagram illustrates the power supply circuit for the PWRCONNP4_BLACK-RH-3. The input is +12VIN, which passes through a fuse (L16, CH1.2u15A1.7m-RH). The circuit then includes a series of capacitors: C657 (0.01u/16V/4), EC71 (270u/16V/3.5's/O), EC84 (270u/16V/3.5's/O), and C659 (X_10u/16V/12). The output is labeled 12VIN. A component JPWR2 is shown with its pin connections.



Size Custom	Document Description VRD12 - RT8859 2+1Phase	Rev 1.0
Date: Tuesday, November 16, 2010	Sheet 28 of 33	

VCCP POWER

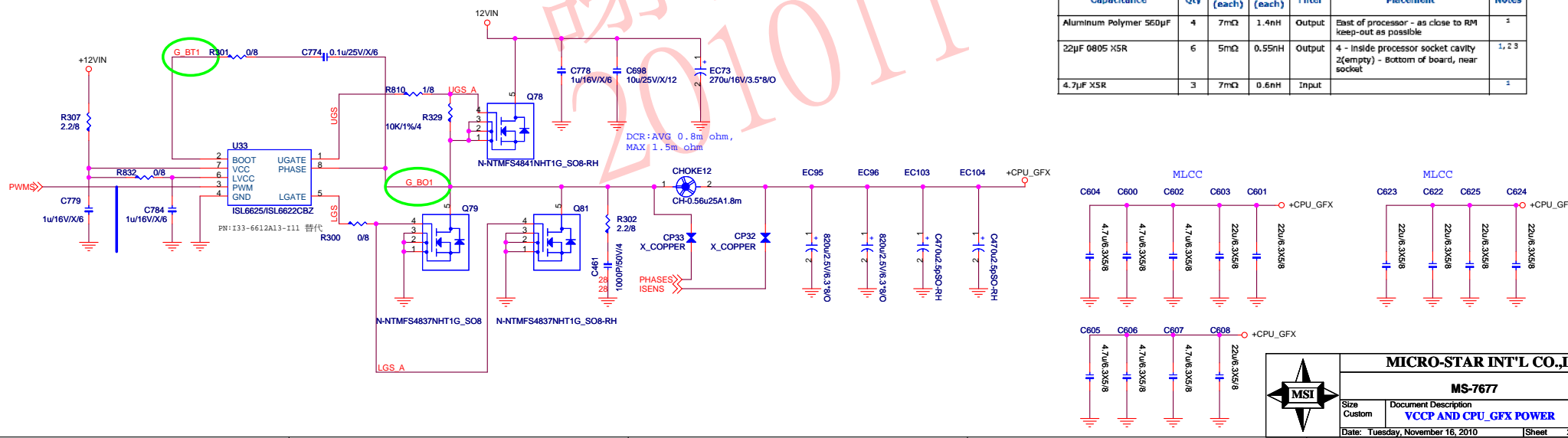


GFX POWER

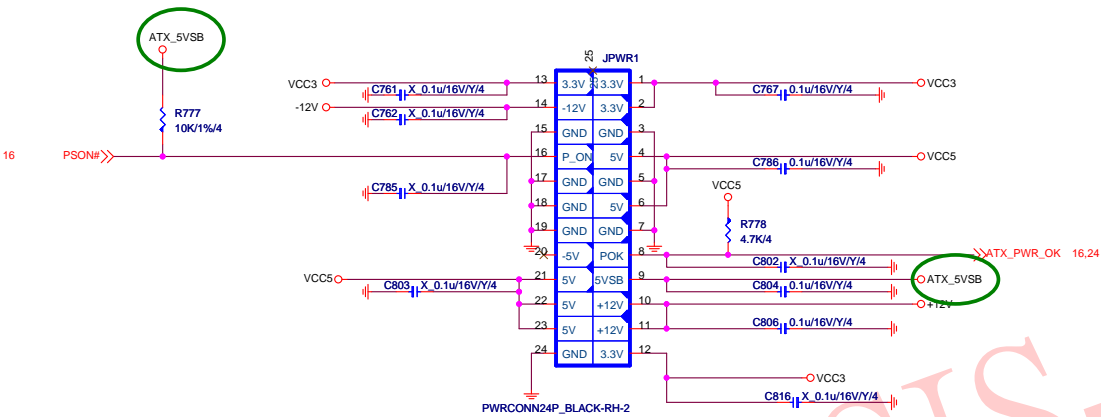
VCCAXG SVID:25A TDC:35A

Table 3-4. VCCAXG Decoupling Requirements

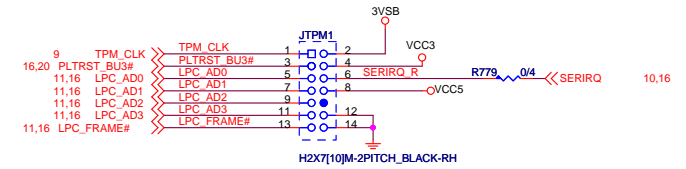
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 XSR	6	5mΩ	0.55nH	Output	4 - Inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF XSR	3	7mΩ	0.6nH	Input		1



ATX POWER CONNECTOR



TPM

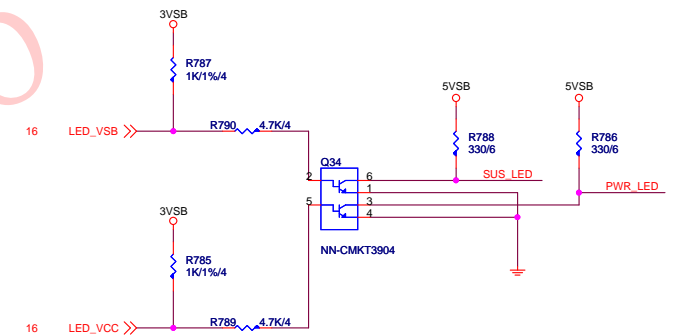


FOR INTEL TEST

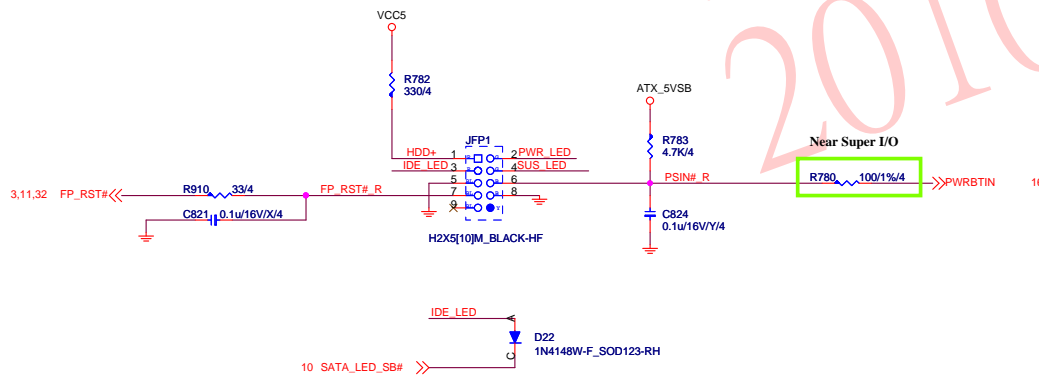


www.aitech1.ru

LED (for Fintek 71882)



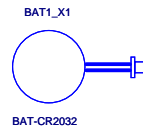
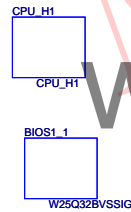
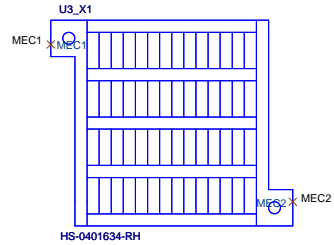
FRONT PANNEL



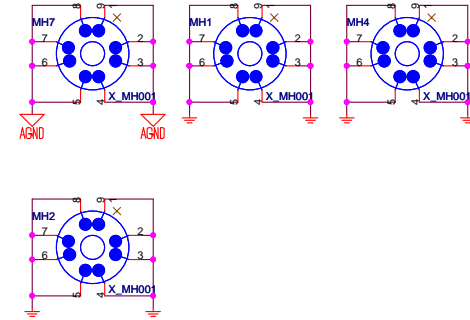


7677-0c

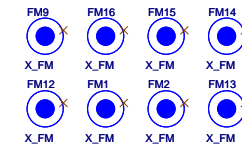
PK0-076770B-K10, 慶生, 10, 寶安恩斯邁廠 (MSIS)
PK0-076770B-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)
PK0-076770B-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)



Mounting Holes



Optical Fiducial Marks-120

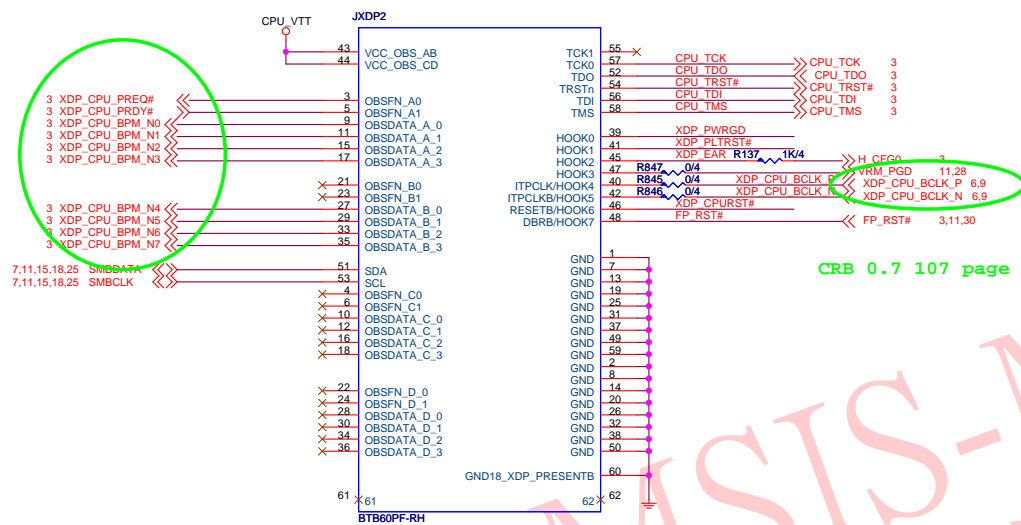


Simulation



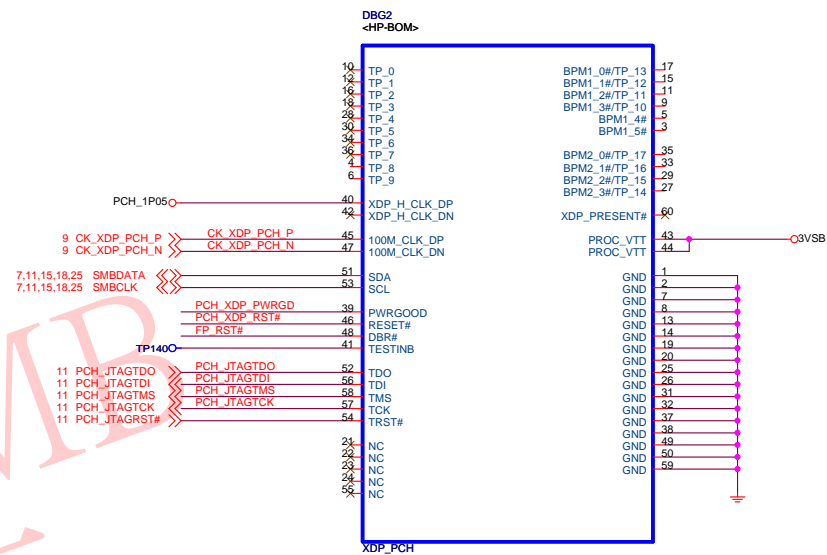
	MICRO-STAR INT'L CO.,LTD		
	MS-7677		
	Size Custom	Document Description Manual Parts	Rev 1.0
	Date: Tuesday, November 16, 2010	Sheet 31	of 33

Reserve debug port 5020

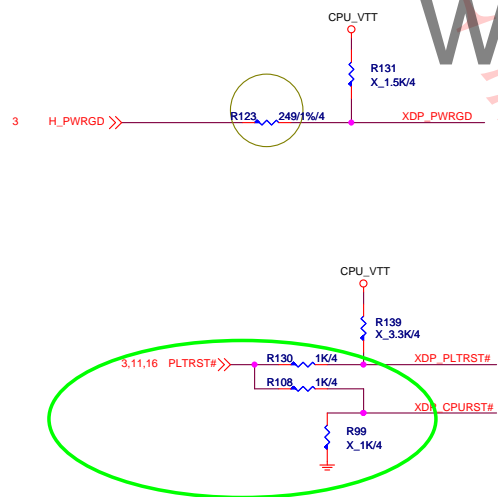


CRB 0.7 107 page

PCH XDP



PCH XDP PWRGD/RESET




MICRO-STAR INT'L CO.,LTD

MS-7677

Size	Document Description
Custom	XDP CPU & CP

Date: Tuesday, November 16, 2010	Sheet 32 of 33
----------------------------------	----------------

MSIS-MB
www.aitech1.ru
謝代燕
20101116

	MICRO-STAR INT'L CO.,LTD			
	MS-7677			
	Size	Document Description	Rev	
	Custom	History	1.0	
	Date: Tuesday, November 16, 2010		Sheet	33 of 33